Docket No.: 50006-111 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
Yoshikado SANEMITSU	:	
Serial No.: 09/902,588	:	Group Art Unit: 2876
Filed: July 12, 2001	:	Examiner: Uyen Chau N. Le

For: PC ADAPTER CARDS AND METHOD OF MANUFACTURING THE SAME

APPEAL BRIEF

Commissioner for Patents
Washington, DC 20231

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed October 17, 2002.

I. REAL PARTY IN INTEREST

Mitsubishi Denki Kabushiki Kaisha is the real party in interest in the pending application.

II. RELATED APPEALS AND INTERFERENCES

No appeal or interference is known to Appellant that will affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-5 remain pending. Claims 1-5, stand under final rejection dated June 19, 2002, from which rejection this Appeal is taken.

IV. STATUS OF AMENDMENTS

Claims 1-5 have not been amended after the Final Office Action dated June 19, 2002.

V. SUMMARY OF INVENTION

In the past, PC cards (or mini-cards) have typically been manufactured by mounting circuit elements on an array of card substrates, separating the substrates and then encasing each of the separated substrates. (See page 1, line 16 - page 2, line 7). Because of the size of each of the separated substrates is approximately that of a postage-stamp, the separated substrates are difficult and time-consuming to handle in the manufacturing process. Embodiments of the present invention, however, relate to a manufacturing method of mini-cards that provides an array of individual substrates connected together, mounting semiconductor devices on each of the individual substrates and then encapsulating the individual substrates with a protective case before dividing the individual substrates t produce individual mini-cards. (See page 2, lines 17-25). Other embodiments of the present invention relate to mini-cards manufactured according to the above-described manufacturing method. While still another embodiment relates to a mini-card having a portion of the substrate exposed through a side of the encapsulating, protective case.

Claims 1, 4 and 5 are the sole independent claims. Claim 4 is presented below with elements read on drawing figures, as urged in MPEP 1206.

4. A mini-card (**10**, FIG. 1D) with a semiconductor memory device (**2**, FIG. 1B) is characterized in that the mini-card is manufactured by a method comprising the steps:

providing an array of substrates including a plurality of individual substrates (**1**, FIG. 1A) connected together (see FIG. 1A);

mounting a semiconductor memory device (**2** or **3**, FIG. 1B) on each of the individual substrates (**1**, FIG. 1A);

covering the individual substrates with respective cases (**5**, FIG. 1C); and

dividing, after the step of covering is completed, the substrate array to provide encased individual substrates each completing the mini-card having the semiconductor memory device embedded therein (see FIG. 1D).

As stated in the section of the Manual noted above, the claims are not to be limited to this embodiment by such reading.

VI. ISSUES

Whether claims 1-5 are unpatentable under 35 USC §103(a) over Hata et al. (US 6,383,835) in view of Mostafazadeh et al. (US 6117,710) and Luvini et al. (US 6,193,557), hereinafter *Hata*, *Mostafazadeh* and *Luvini*, respectively.

VII. GROUPING OF CLAIMS

The appealed claims do not stand or fall together as a group. Claims 1, 2, 3 and 4 stand or fall as a group and claim 5 stands or falls separately.

VIII. THE ARGUMENT

The factual determination that any of claims 1-5 are unpatentable under 35 USC §103(a) over *Hata* in view of *Mostafazadeh* and *Luvini* is erroneous given the differences between these claims and the applied combination of references and the lack of motivation to combine the references as proposed by the Examiner.

All claims on appeal have been rejected under 35 U.S.C. §103(a). Legal precedent is well developed on this subject. In the application of a rejection under 35 U.S.C. §103, it is incumbent upon the examiner to factually support a conclusion of obviousness. *In re Mayne,* 104 F.3d 1339, 41 USPQ2d 1451 (Fed. Cir. 1997*); In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). As stated in *Graham v. John Deere Co.* 383 U.S. 1, 13, 148 USPQ 459, 465 (1966), obviousness under 35 U.S.C. §103 must be determined by considering (1) the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims in issue; and (3) resolving the level of ordinary skill in the pertinent art. The PTO is thus charged with the initial burden of identifying a source in the applied prior art for: (1) claim features; and (2) the realistic requisite motivation for combining applied references to arrive at the claimed invention with a reasonable expectation of successfully achieving a specific benefit. *Smith Industries Medical Systems v. Vital Signs,* 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999). This burden is not met if there is no showing that the combination of references would actually meet all the limitations of the claims under consideration.

The examiner must provide a reason why one having ordinary skill in the art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985); *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967). The examiner should recognize that even if the prior art *could* be modified so as to result in the

combination defined by the claims the modification would not have been obvious unless the prior art suggested the desirability of the modification. *In re Deminski*, 796 F.2d 436, 230 USPQ 313 (Fed. Cir. 1986). In the absence of such a prior art suggestion for modification of the references, the basis of the rejection is no more than inappropriate hindsight reconstruction using appellant's claims as a guide. *In re Warner*, 379 F.2d 1011, 154 USPQ 173 (CCPA 1967).

What may or may not be known in general does not establish the requisite realistic motivation. *In re Deuel*, 51 F.3d 1552, 34 USPQ2d 1210 (Fed. Cir. 1995). The requisite motivation to support the ultimate legal conclusion of obviousness under 35 U.S.C. §103 is not an abstract concept, but must stem from the applied prior art as a whole and have realistically impelled one having ordinary skill in the art, at the time the invention was made, to modify a reference in a specific manner to arrive at a specifically claimed invention with a reasonable expectation of achieving a specific benefit. *In re Newell,* 891 F.2d 899, 13 USPQ2d 1248 (Fed. Cir. 1989). It is submitted that the examiner has not discharged the burden of establishing obviousness.

Independent claim 1 is reproduced below as follows:

1. A method of manufacturing a mini-card with a semiconductor memory device comprising the steps of:

providing an array of substrates including a plurality of individual substrates connected together;

mounting a semiconductor memory device on each of the individual substrates;

covering the individual substrates with respective cases; and

dividing, after the step of covering is completed, the substrate array to provide encased individual substrates each completing the mini-card having the semiconductor memory device embedded therein.

Claims 1 - 4 require "an array of substrates including a plurality of individual substrates connected together" and "covering the individual substrates with respective cases." In direct contrast, *Hata* teaches a single, large substrate (1, FIG. 9A) that can accommodate multiple circuits. The figures in *Hata* such as 7B, 9B and 13B are merely partial views of portions of this single substrate (1) in order

to show finer detail. Thus, *Hata* teaches a single substrate (1) having multiple circuit areas which is covered by a uniform coating of resin (6). The sealing resin (6) covers apparently the entire substrate (1) and does not require determining a coverage area or the use of mold frames (see column 7, lines 22-26).

Hata, therefore, does not disclose the array of individual substrates recited in claims 1 and 4, each of which are covered with a respective case.

Mostafazadeh does not teach nor suggest a plurality of individual substrates used in a mini-card or in making a mini-card; instead, *Mostafazadeh* relates to a single conventional integrated circuit (IC) package. In its background section, *Mostafazadeh* describes an individual prior-art IC package in which a die is covered with a plastic casing. Thus, *Mostafazadeh* does not disclose the claim elements identified above which are missing from the disclosure of *Hata* because *Mostafazadeh* does not teach nor suggest (a) a plurality of individual substrates in an array nor (b) covering each of a plurality of individual substrates in an array with a respective case.

Luvini relates to an improved electrical connector for mini-cards that reduces the number of components needed to establish an electrical connection between the card and a circuit board. (See Column 4, lines 16-21). In describing this connector, *Luvini* describes various mini-cards and their uses but does not suggest a mini-card manufacturing process involving a plurality of individual substrates, each of which is covered by a respective case nor mini-cards manufactured using such a process.

As each of the references fail to disclose or suggest (a) a plurality of individual substrates in an array and (b) covering each of a plurality of individual substrates in an array with a respective case, the combination of references does not disclose nor suggest all the limitations recited in claims 1 and 4. The above-argued differences between the claimed inventions recited in claims 1 and 4 and the

combination of *Hata* in view of *Mostafazadeh* and *Luvini* preclude the factual determination that the combination of these references provide a prima facie basis to deny patentability, within the meaning of 35 USC §103, of claims 1 and 4 and claims which depend therefrom.

Independent of the above arguments, Appellant urges that one of ordinary skill would not have been motivated to combine the teachings of *Mostafazadeh* and *Hata*. In particular, *Mostafazadeh* discloses that encapsulating an integrated circuit (as shown in FIG. 1) is an undesirable goal. At column 1, line 66 - column 2, line 10, *Mostafazadeh* explicitly teaches away from enclosing a circuit in a case for thermal reasons (see also, column 1, lines 42-45). Thus, one of ordinary skill would not have been realistically motivated to ignore the warnings, and explicit teachings, of *Mostafazadeh* to modify the devices of *Hata* to have top and bottom case segments.

In addition, the devices of *Hata* are surface mounted ICs. In FIG. 8, for example, the bottom portion of lead (2a) must be left uncovered to connect to whatever circuit board the substrate (1a) is eventually mounted on. Encapsulating these leads of *Hata* with top and bottom case segments (as purportedly taught by *Mostafazadeh*) would render the device of *Hata* unsuitable for its purpose and make it ineffective because its electrical connectors would be covered. Thus, one of ordinary skill would not have been realistically motivated to combine the teachings of *Hata* and *Mostafazadeh* as suggested by the Examiner because doing so would result in an inoperative device.

Additionally, the motivation provided by the Examiner is illusory. Within *Hata*, the resin (6) covers the top of circuit board (1) in order to protect the chip (4). Additionally, the through holes on the board (1) are covered with insulating film (3). (see column 5, lines 1-6). Thus, in the arrangement of *Hata*, the chips (4) are already protected from contamination which is the exact benefit that the Examiner argued would be realized by modifying *Hata* in view of *Mostafazadeh*. Appellant respectfully contends that the Examiner's explanation of why one of ordinary skill would be motivated to

combine these two references is merely a conclusory statement that is not founded on any specific teachings in either of the references. *Hata* already includes a mechanism for protecting circuit elements. Thus, one of ordinary skill would have had no realistic motivation to modify *Hata* to include an individual case segment for each individual substrate (purportedly taught by *Mostafazadeh*) because such modification of *Hata* is unnecessary and provides no additional benefit.

For at least any of these reasons, and contrary to the Examiner's contentions, Appellant urges that one of ordinary skill would not have been realistically motivated to combine the teaching of *Hata* and *Mostafazadeh* as suggested by the Examiner. Without the requisite showing of why one of ordinary skill would have been realistically impelled to undertake the proposed modification to *Hata* in view of *Mostafazadeh*, a prima facie basis to deny patentability, of claims 1 and 4, under 35 USC §103 has not been properly established. As claims 2 and 3 depend from claim 1 and include all the limitations of that claim, a prima facie basis to deny patentability, of claims 2 and 3, under 35 USC §103 also has not been properly established.

Independent of the above arguments, Appellant urges that one of ordinary skill would not have been motivated to combine the teachings of *Mostafazadeh* and *Hata* with those of *Luvini* as suggested by the Examiner. The purported benefit gained from *Luvini* is that the IC packages of both *Hata* and *Mostafazadeh* would be made smaller if the teachings of *Luvini* were used to modify *Hata* and *Mostafazadeh*. While Appellant acknowledges that none of the references explicitly discuss specific sizes of the circuitry involved in each disclosure, the Examiner's basis for combining the references appears to be factually incorrect if *Hata* and *Mostafazadeh* are assumed to relate to conventionally-sized IC packages. Appellants urge that putting IC packages within a mini-card housing would not make a more compact system as contended by the Examiner. To the contrary, the resulting mini-card would be less compact than an IC package taught by *Hata* and *Mostafazadeh*. Accordingly, Appellant

urges that the Examiner has not discharged the burden of providing the specific motivation, based on factual findings, required to establish a prima facie basis to deny patentability. Without the requisite showing of why one of ordinary skill would have been realistically impelled to undertake the proposed modification to *Hata* in view of *Mostafazadeh* and *Luvini*, a prima facie basis to deny patentability, of claims 1 - 4, under 35 USC §103 has not been properly established.

Claim 5 recites a semiconductor memory device on a substrate and requires that a case cover the substrate and that a part of the substrate be exposed to an external side of the case, as described, for example, at page 7, lines 7-11 with respect to FIG. 3.

Appellant urges that the combination of *Hata*, *Mostafazadeh*, and *Luvini* do not disclose nor suggest all these claim features. An example of the devices of *Hata* is shown in FIG. 8; the other embodiments are substantially similar. Within *Hata*, the resin (6) or "case" sits on top of substrate (1a) such that all 4 sides of the case are exposed. However, there is no portion of the substrate which is exposed to a side of this case (6) as recited in claim 5. More particularly, the sides of the case (6) are above the substrate (1a) and the insulating film (3) covers any portion of the substrate (1a) that is near the sides of resin (6). Thus, within *Hata*, it is physically impossible for an aperture or opening (if it were even present in *Hata*) in the side of the case (6) to effect exposure of the substrate (1a) as recited in claim 5. Neither *Mostafazadeh* nor *Luvini* disclose or suggest exposure of a substrate from the side of an encapsulating case and, therefore, the combination of these references does not disclose nor suggest every limitation recited in claim 5. Thus, the combination of references does not provide the requisite factual basis to establish a prima facie case to deny patentability of claim 5 under 35 USC §103.

For at least the reasons explained above with respect to claims 1 - 4, Appellant also urges that one of ordinary skill would not have been motivated to combine the teachings of *Mostafazadeh*, *Luvini*

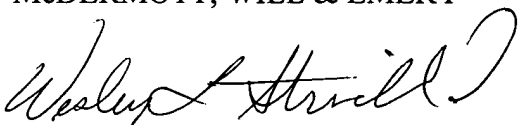
and *Hata* as suggested by the Examiner in rejecting claim 5. Without the requisite showing of why one of ordinary skill would have been realistically impelled to undertake the proposed modification to *Hata* in view of *Mostafazadeh* and *Luvini*, a prima facie basis to deny patentability, of claim 5, under 35 USC §103 has not been properly established.

IX. CONCLUSION

For the reasons advanced above, Appellant urges that the Examiner did not establish a prima facie basis to deny patentability to claims 1-5 under 35 USC §103 over *Hata, Mostafazadeh* and *Luvini*. Appellant, therefore, respectfully solicits the Honorable Board to **reverse** each of the Examiner's rejections.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0417 and please credit any excess fees to such deposit account.

Respectfully submitted,
McDERMOTT, WILL & EMERY



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X. APPENDIX

1. A method of manufacturing a mini-card with a semiconductor memory device comprising the steps of:

providing an array of substrates including a plurality of individual substrates connected together;

mounting a semiconductor memory device on each of the individual substrates;

covering the individual substrates with respective cases; and

dividing, after the step of covering is completed, the substrate array to provide encased individual substrates each completing the mini-card having the semiconductor memory device embedded therein.

2. The method of manufacturing a mini-card with a semiconductor device according to claim 1, wherein, during the covering step, each substrate is sandwiched between top and bottom case segments.

3. The method of manufacturing a mini-card with a semiconductor device according to claim 1, wherein, during the covering step, each substrate is molded into case.

4. A mini-card with a semiconductor memory device is characterized in that the mini-card is manufactured by a method comprising the steps:

providing an array of substrates including a plurality of individual substrates connected together;

mounting a semiconductor memory device on each of the individual substrates;

covering the individual substrates with respective cases; and

dividing, after the step of covering is completed, the substrate array to provide encased individual substrates each completing the mini-card having the semiconductor memory device embedded therein.

5. A mini-card with a semiconductor memory device comprising:

a substrate;

a semiconductor memory device mounted on the substrate; and

a case covering the substrate;

wherein a part of the substrate is exposed to an external side of the case.